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FAQs — Frequently asked questions about HP UPS Management Module

Newsletter staff recently received questions from the field regarding a previous newsletter article on HP UPS Management Module (HPMM) (refer to ISS Technology Update Volume 6, Number 8). Since other customers may be experiencing the same issues, this brief article will present those questions. HP technical staff has provided the answers.

FAQs

Question #1

- Q.** Is there a version of the HP UPS Management Agent available for customers running operating system ESX 3.0.x that will provide an automatic shutdown solution when the uninterruptible power supply (UPS) runs out of power? We found compatibility information online for VMware 2.5.x, but not specifically for 3.0.x.
- A.** Technically, the current HPMM Power Protection Agent should work with VMware 2.5.x or ESX 3.0.x. The only difference is that for ESX 3.0.x there is a shutdown option. If this option is not set correctly, when the server is rebooted, the user will receive an error message at the login screen because the server was not shut down gracefully.

Question #2

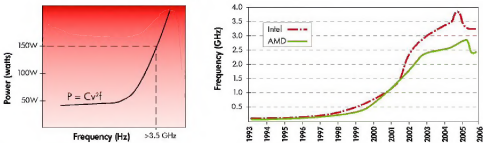
- Q.** From where can the agent be downloaded, either internally or externally? We can find Windows, HP-UX, and Linux versions online externally, but none for ESX (even version 2.5.4).
- A.** VMware is based on Linux; the Linux agent is available for download at <http://h18004.www1.hp.com/products/servers/proliantstorage/power-protection/software/module/ups/dl.html>

Count on the number of CPU cores increasing

What's driving the increase in core counts?

Historically, the hunger for higher performance has driven major processor innovations. With traditional single-core CPUs, improved performance is possible by increasing the clock frequency and increasing the number of transistors. But increasing the clock frequency leads to greater power consumption and heat generation. Processor power consumption (P) has a linear relationship to clock frequency (f) and a non-linear relationship to the supply voltage (v), as expressed by the equation $P = Cv^2f$, where the total capacitance, C , is proportional to the number of transistors. As the frequency increases, there is an exponential increase in CPU power use (Figure 1 left) because within a particular transistor geometry generation, more voltage must be applied to get transistors to switch on and off at higher frequencies. At higher voltages, transistors experience increased leakage current—current that takes alternate paths through the transistor—resulting in increased heat generation and less efficient operation. From a power perspective, processors are more efficient when they operate below their maximum frequency. This fact combined with constrained facility space and rising power and cooling costs, has caused the market to demand higher CPU performance per watt. This market shift is driving processor vendors to shrink the size of cores. Smaller cores require less power, permitting more cores to be built into a single processor to get more performance out of each silicon chip.

Figure 1-1. Power use and heat dissipation increase exponentially with frequency (left), so after 2004, processor vendors began limiting the frequency (right) and increasing the number of cores per chip.



What determines the number of CPU cores offered in HP ProLiant servers?

HP ProLiant servers include a range of single-core and multi-core processors from Intel and AMD. In determining which processor to offer for each ProLiant server model, HP tries to match the needs of its customers with the processor options available from these two processor vendors. The processor vendors determine the number of processor cores to offer by evaluating market trends while trying to maintain a competitive advantage.

Are more cores better?

Based on performance-per-watt, low-voltage quad-core processors deliver a cooler and more power-efficient option than processors with fewer cores. However, to take advantage of multiple cores, multi-threaded applications need to be employed. When more multi-threaded applications became available, HP recommends that customers begin to migrate from legacy applications to benefit from the higher performance and increased power efficiency. Alternatively, there are methods to shut down underutilized cores or place them in a low-power state to provide investment protection for tomorrow (see "Optimizing the performance of multi-core processors" in this issue).

Additional resources

For additional information on the topics discussed in this article, visit:

Resource	URL
"The AMD processor roadmap for industry standard servers, 5th edition" technology brief	http://h20000.www2.hp.com/bc/docs/support/SupportManual/c00428708/c00428708.pdf
"Intel processor roadmap for industry standard servers, 8th edition" technology brief	http://h20000.www2.hp.com/bc/docs/support/SupportManual/c00164255/c00164255.pdf

Optimizing the performance of multi-core processors

As processor vendors stretch the boundaries of physics to increase the number of cores on a single die, small-to-medium businesses and enterprise customers need to have a strategy to fully utilize the available cores. By all accounts, the trend to increase the number of cores per chip is irreversible because single-core CPUs use more power to achieve the performance levels of multi-core CPUs. Multi-core CPUs are designed to stay busier and operate at a lower frequency than a single-core processor which results in higher performance per watt. The power savings and performance improvements of multi-core technology are essential to the evolution of the entire computer industry.

Key technologies that enable customers to take advantage of multi-core CPUs include virtualization and parallel processing. Virtualization technology transforms a single physical server into multiple virtual machines (VMs), allowing the server's physical resources (memory space and I/O devices) to service multiple guest operating systems. In doing so, virtualization technology increases hardware utilization, thereby lowering the total cost of ownership of servers and reducing the number of servers required.

In parallel processing, multithreaded applications are executed in parallel on multiple cores. The availability of multi-threaded applications has been delayed by the changes required from the software programmers and vendors. Programmers must adopt parallelization techniques and must recode existing applications or code new ones from scratch. Software vendors must consider new business models other than the traditional method of charging customers a license fee for each server or processor that runs an application. These factors may have slowed the development of multi-threaded software, but they are not slowing down processor vendors—quad-core CPUs are on the market now and massive multi-core CPUs (with 16+ cores) will be available in a few years.

Customers have at least two options in instances where they cannot use all of the available cores. One option is to shut down one or more cores and allocate that power to the remaining cores. It is more energy efficient to speed up the remaining cores while staying within the processor's thermal design power (TDP). Another option is to reduce the processor's power consumption to match the application requirements. If customers choose to reduce processor power use, they should be aware that the potential energy savings may be negated by the increased inefficiency of the power supply at decreased loads. This tactic requires power supplies that are efficient at lower loads.

By using a BIOS setup option or an OS boot-loader option, customers may statically choose to disable some of the cores within a multi-core CPU at boot time. An operating system or a virtual machine manager (VMM), such as hypervisor, may be used to dynamically disable processor cores and readjust processor P-states (performance states) to appropriately reallocate power to the remaining cores.

Additional resources

For additional information on the topics discussed in this article, visit the following:

Resource	URL
"Integrated hypervisor virtualization technologies in HP BladeSystem ProLiant server blades and ProLiant servers" technology brief	http://h20000.www2.hp.com/bc/docs/support/SupportManual/c01518167/c01518167.pdf

Meet the Expert — Kim Sides

Kim Sides has had a fruitful 20-year career with Industry Standard Servers (ISS). She has achieved the level of ISS Master Technologist by demonstrating dedication, innovation, and excellence in her work. As the speed and complexity of designs have increased, Kim has been on the forefront of using new tools and techniques to improve signal integrity (SI) analysis.

She is known as an unselfish team player whose soft-spoken and kind demeanor are balanced by her intelligence and resolve. Her expertise is even sought out by other HP engineers because of her willingness to help others to learn.

According to Ken Jansen, her manager, "Nothing ever seems to faze her. She just looks at the job that needs to be done, determines the best way to do it, and gets after it." Ken said that in the almost 21 years that he has known Kim, he can never remember seeing her get flustered. Kim achieves "balance" between body and mind through her two hobbies: swimming and studying the Bible.

Kim and Jim, her husband, have been married for 21 years and have a son (20) and a daughter (18). Below are excerpts from a conversation with Kim.



Name: Kim Sides
Title: Master Technologist - TGS ESS ISS
Shared Engineering Services
Years at HP: 20
University/Degree

- Louisiana State University: BSEE 1979
- University of Houston: MSEE 1987

U.S. Patents: 8

Why did you decide to become an engineer?

Kim: I was fascinated with a Basic Electrical Circuit course that I took in 8th grade. During that class, I realized how mathematics can be used to solve real physical problems, so I decided to be an electrical engineer.

What is your favorite invention or most interesting research?

Kim: My most interesting research was the Signal Integrity Etch Test Vehicle that I collaborated on with the Digital SI engineers and Metrology lab in 2002. Up to that time, we never had a test vehicle that would enable us to extract loss tangent data as a function of frequency. The Signal Integrity Etch Test Vehicle enabled us to extract the loss tangent of PCB material and correlate between measurement and simulation for transmission line losses on printed wiring board copper traces. During this project, I discovered the fiber weave effect in signal integrity of a differential pair of transmission line. The differential pairs on our test vehicle were designed to have maximum of 0.18 picoseconds (ps) in-pair skew (difference in propagation delay between the two traces), but in the lab we found there was up to 59 ps in-pair skew in some differential pairs. This large skew significantly reduced signal quality of the differential transmission lines. Using simulation and measurement data, we proved that the unexpected skew was due to non-homogenous PCB dielectric material. PCB dielectric material is a mixture of resin and fiberglass weave fabric. Fiberglass has much higher dielectric constant than resin, so if one trace is routed over the fiber weave and the other trace is not, then there will be a difference in velocity between the two traces. Today, we route all differential high-speed signals at an angle to mitigate the in-pair skew due to the fiber weave effect.

How much customer input goes into the design of your products?

Kim: I don't have direct contact with customers, so I get customer input by working with the product groups. Customers want reliable, innovative, and cost-effective products. I take these criteria seriously in my signal integrity work.

What must HP do to remain the leader in industry-standard servers?

Kim: I believe that HP should continue to increase investment in research and development in the areas of signal integrity and power integrity. In order to produce servers that operate reliably at multi-gigahertz speed, we must expand our knowledge and experience in these areas. This requires us to accurately model and simulate high-speed channels and power distribution networks.

Common SM CLP scripting commands for ProLiant server management

This is the first in a series of articles that discuss common SM CLP (Server Management Command Line Protocol) scripting commands. SM CLP is one of the communication, or access, protocols that can be used with the Systems Management Architecture for Server Hardware (SMASH).

Some customers want to use scripts to perform basic target operations on ProLiant servers (for instance, powering on or powering off the server, or obtaining event logs). From a Windows or Linux client, administrators can use SM CLP to remotely interrogate and control servers using the Integrated Lights-Out 2 (iLO 2) processor.

SMASH/CLP is accessed using Secure Shell (SSH). SSH can be interactive (as in a shell) or it can execute in a "command" mode by processing a single command at a time. The following examples demonstrate SSH command mode using Plink, a Windows utility that provides SSH command line support. Plink and PuTTY executables, source code, and license terms are freely distributed on the web. Other SSH command line utilities should support this functionality in a similar manner.

The following examples specify user credentials on the command line. If user credentials are not specified, iLO 2 prompts for account credentials, interrupting the process. iLO 2 also supports SSH key-based authentication.

Check the power status of the machine

The "show system1" command returns the property "enabledstate" as the power state in SM CLP terminology.

```
C:\putty>plink -ssh -l admin -pw password ilo2system.corp.net show system1
enabledstate | grep  enabledstate

show system1 enabledstate

enabledstate=enabled
```

Power-on the server

If the server is off, the "start system1" command issues a virtual power button press.

```
C:\putty>plink -ssh -l admin -pw password ilo2system.corp.net start system1

start system1
status=0
status_tag=COMMAND COMPLETED
Server power on.
</>hpiLO->
```

Power-off the server

If the server is on, the "stop system1" command issues a virtual power button press. This event is normally intercepted by the OS ACPI support to initiate a graceful shutdown. It may be ignored if the OS is configured to ignore graceful shutdown requests, if the OS is hung up, or if an OS driver is waiting on a completion status. If this is the case, then the "-force" parameter can be used to cause a hard shutdown.

```
C:\putty>plink -ssh -l admin -pw password ilo2system.corp.net stop system1

stop system1
```

```
status=0  
status_tag=COMMAND COMPLETED  
Server power off.  
</>hpILO->
```

Power cycle the server

The "reset system1" command, as shown below, performs a reset by power cycling the server, regardless of the OS state.

```
C:\putty>plink -ssh -l admin -pw password ilo2system.corp.net reset system1  
  
reset system1  
status=0  
status_tag=COMMAND COMPLETED  
Resetting server.  
</>hpILO->
```

Additional resources

For additional information on the topics discussed in this article, visit:

Resource	URL
HP Integrated Lights-Out	www.hp.com/go/ilo
DMTF SMIASH information	www.dmtf.org/standards/mgmt/smash/
PUTTY and Plink	www.google.com/search?q=PUTTY

Recently published industry standard server technology communications

Title	URL
"Managing HP BladeSystem c-Class Systems" technology brief, 2nd edition	http://h20000.www2.hp.com/bc/docs/support/SupportManual/c00814176/c00814176.pdf
"Deploying HP KVM consoling solutions" technology brief, 2nd edition	http://h20000.www2.hp.com/bc/docs/support/SupportManual/c00793971/c00793971.pdf
"Deploying HP serial consoling solutions" technology brief, 2nd edition	http://h20000.www2.hp.com/bc/docs/support/SupportManual/c01080873/c01080873.pdf
"Implementing Microsoft Windows Enterprise Business Server Release Candidate 1 (RC1) on HP ProLiant servers" integration note	http://h20000.www2.hp.com/bc/docs/support/SupportManual/c01467895/c01467895.pdf
"Implementing Microsoft Windows Small Business Server Release Candidate 1 (RC1) on HP ProLiant servers" integration note	http://h20000.www2.hp.com/bc/docs/support/SupportManual/c01479108/c01479108.pdf
"Power Capping for ProLiant Servers" technology brief	http://h20000.www2.hp.com/bc/docs/support/SupportManual/c01549455/c01549455.pdf
"Technologies for HP ProLiant 100-series servers" technology brief 2nd edition	http://h20000.www2.hp.com/bc/docs/support/SupportManual/c01362433/c01362433.pdf

Industry standard server technical communications can be found at www.hp.com/servers/technology.

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